High Performance Synchronous Buck EVM Using the TPS51125

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1 Introduction

The TPS51125 is a cost effective, dual-synchronous buck controller targeted for notebook system power supply solutions. It provides 5-V and 3.3-V LDOs and requires few external components. The 270-kHz VCLK output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the main converter's efficiency. The TPS51125 supports high-efficiency, fast transient response and provides a combined power-good signal. Out-of-Audio™ mode light-load operation enables low acoustic noise at much higher efficiency than conventional forced PWM operation. Adaptive on-time D-CAP™ control provides convenient and efficient operation. The part operates with supply input voltages ranging from 5.5 V to 28 V and supports output voltages from 2 V to 5.5 V.

TPS51125EVM evaluation module is a high efficiency, dual synchronous buck converter providing 5 V at 8 A and 3.3 V at 8 A from 8-V to 25-V input.

2 Performance Specification Summary

Table 1 gives the EVM performance specifications and qualifications.

Table 1. Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input voltage range	Voltage applied to VBAT	8		25	V
CHANNEL1						
V_{OUT}	Output voltage			5		V
f	Operating frequency	$V_{TONSEL} = V_{VREF}$, V_{VIN} = 12 V, I_{OUT} = 6 A		245		kHz
I_{OUT}	Output current	8 V ≤ V_{VIN} ≤ 25 V	8			A
I_{OC}	Overcurrent limit	V_{VIN} = 12 V		10		
CHANNEL2						
V_{OUT}	Output voltage			3.3		V
f	Operating frequency	$V_{TONSEL} = V_{VREF}$, V_{VIN} = 12 V, I_{OUT} = 6 A		305		kHz
I_{OUT}	Output current	8 V ≤ V_{VIN} ≤ 25 V	8			A
I_{OC}	Overcurrent limit	V_{VIN} = 12 V		10		

3 Schematic

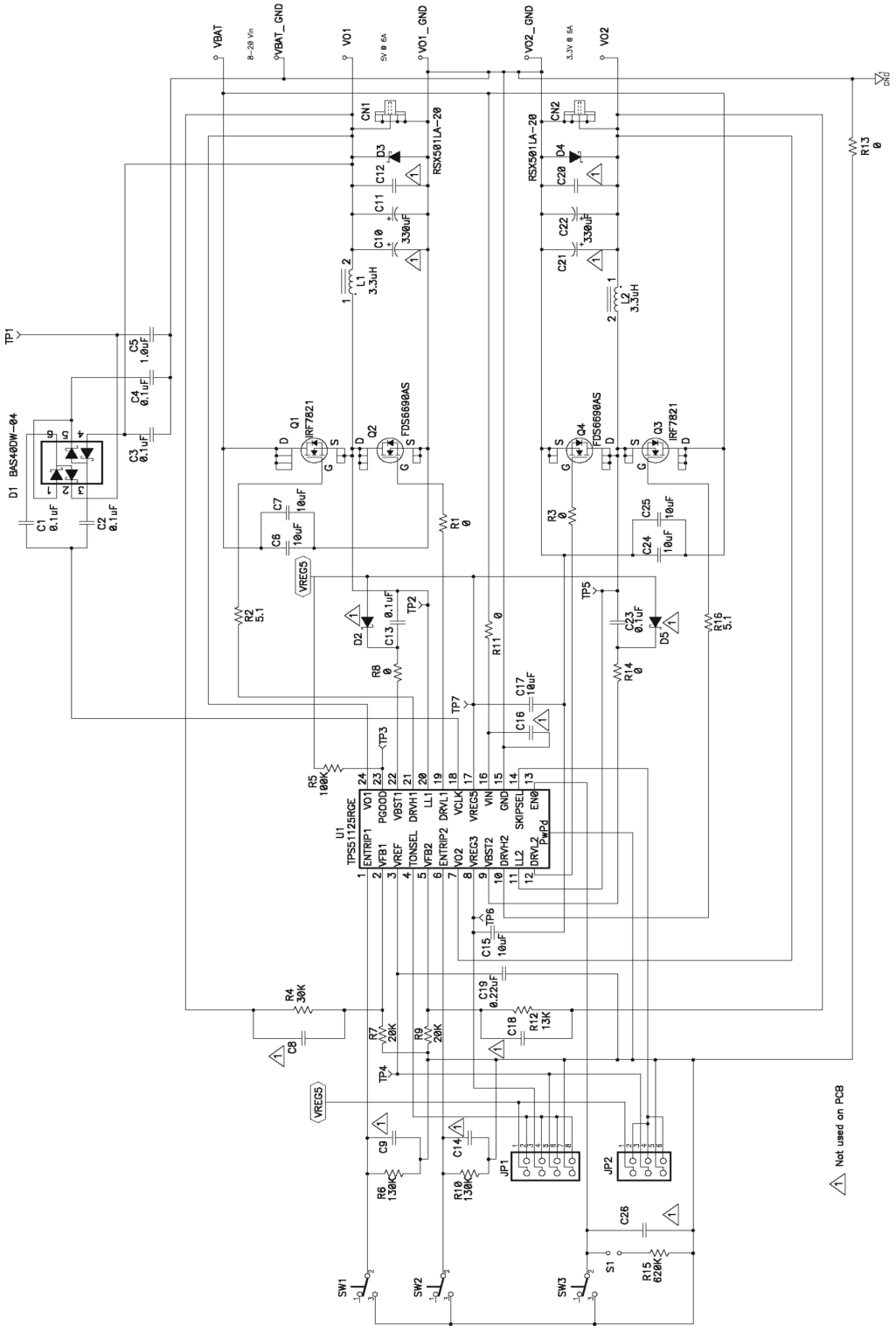

Figure 1. TPS51125-EVM Schematic Diagram

4 Test Setup and Results

4.1 Test Setup

Connect test equipment and TPS51125EVM board as shown in Figure 2.

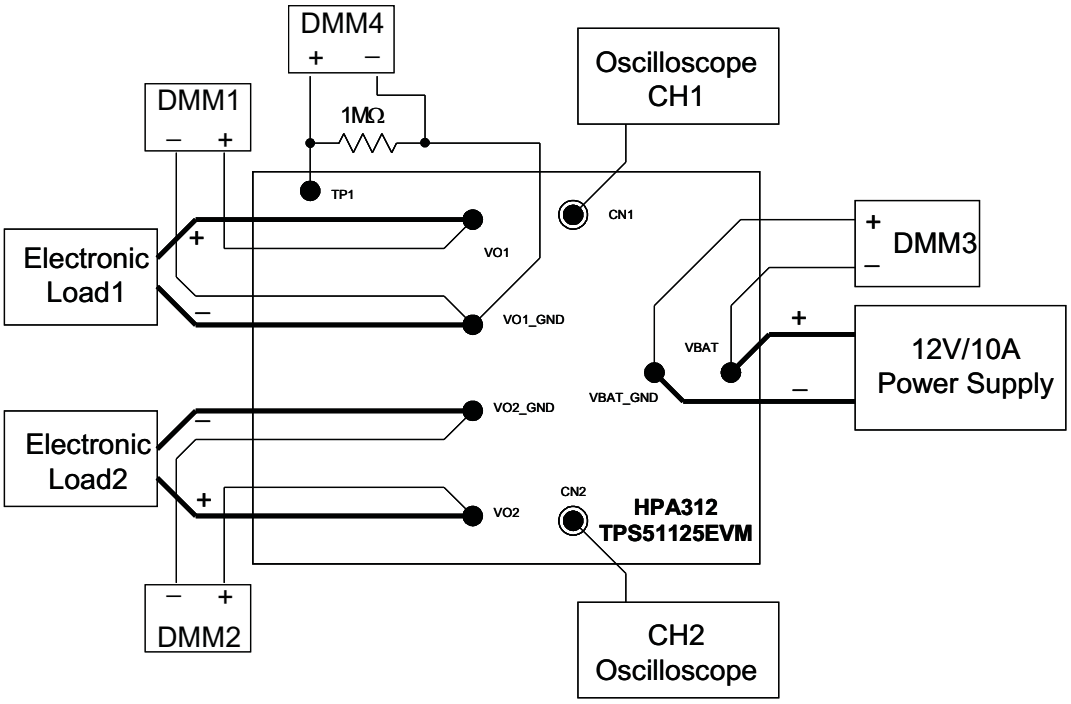

Figure 2. Equipment Setup for TPS51125EVM board

4.2 Test Procedure

1. Ensure the switches SW1 (ENTRIP1), SW2 (ENTRIP2) and SW3 (EN0) are in “OFF” position.
2. Ensure the shunt jumper for JP1 is set 5-pin to 6-pin (Med1), and shunt jumper for JP2 is set 3-pin to 4-pin (Auto-skip).
3. Apply appropriate VBAT voltage to VBAT and VBAT_GND terminals.
4. Turn on SW3 (EN0), and both VREG5 (5V-LDO) and VREG3 (3.3V-LDO) start up.
5. When SW3 stays on, VREF (2V-REF) enables.
6. When SW3 stays on and turn on SW1 (ENTRIP1), CH1-output starts up.
7. When SW3 stays on and turn on SW2 (ENTRIP2), CH2-output starts up.

4.3 Start-Up Performance

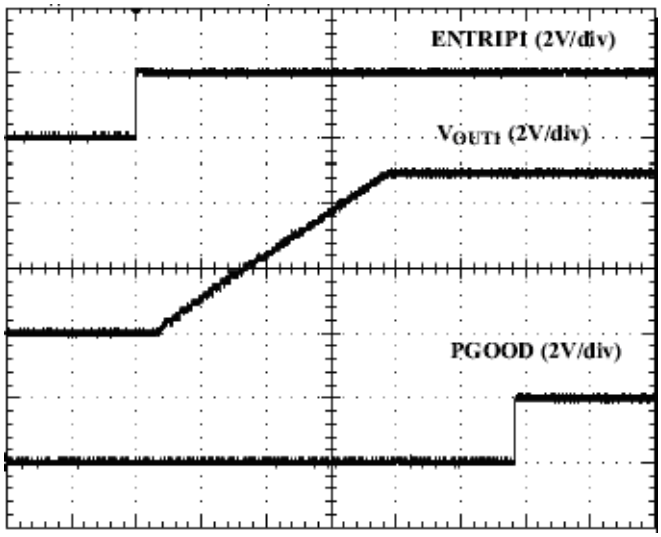

Figure 3. 5-V Startup Waveforms

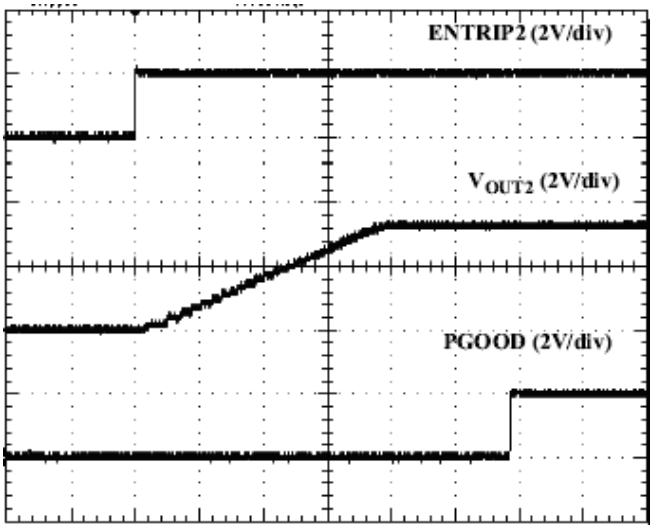

Figure 4. 3.3-V Startup Waveforms

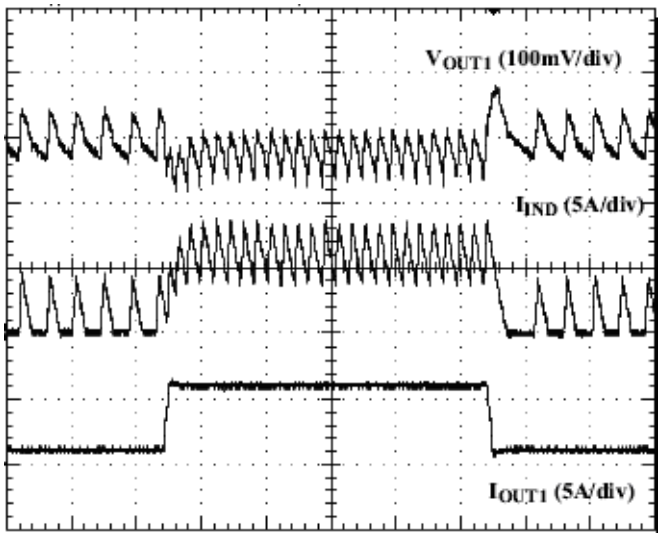

Figure 5. 5-V Load Transient Response

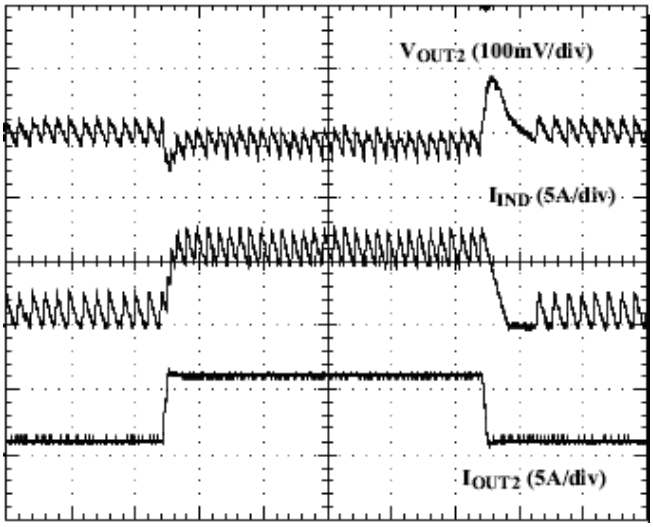

Figure 6. 3.3-V Load Transient Response

5 Configuration

This EVM can be set at a configuration of the user's choice. Please refer to the following specific configuration setting sections

5.1 Switching Frequency Selection

The switching frequency can be set by the TONSEL pin using JP1 on the EVM. The default setting is 245 kHz for CH1 and 305 kHz for CH2.

Table 2. Switching Frequency Selection

TONSEL CONNECTION	SWITCHING FREQUENCY (kHz)	
	CH1	CH2
GND (SLOW)	200	250
VREF (MED1)	245	305
VREG3 (MED2)	300	375
VREG5 (FAST)	365	460

5.2 Operation Mode Selection

Operation mode can be set by the SKIPSEL pin using JP2 on the EVM. The default setting on the EVM is auto-skip mode.

Table 3. Operation Mode Selection

SKIPSEL CONNECTION	OPERATION MODE
GND	PWM only
VREF	Auto skip
VREG5	Out-of-Audio™

5.3 VCLK ON/OFF Selection

The VCLK drive for the charge-pump can be disabled by pulling down EN0 with 620 kΩ of resistance using S1 on the EVM.

Table 4. VLCK Control

END CONNECTION	VCLK
OPEN	ENABLED
Pull down to GND with 620 kΩ	DISABLED

6 Physical Layouts

This section provides the board layout and assembly drawings for the EVM, that include the top layer (Figure 7), the bottom layer (Figure 8), and inner layer views (Figure 9 and Figure 10) of the EVM.

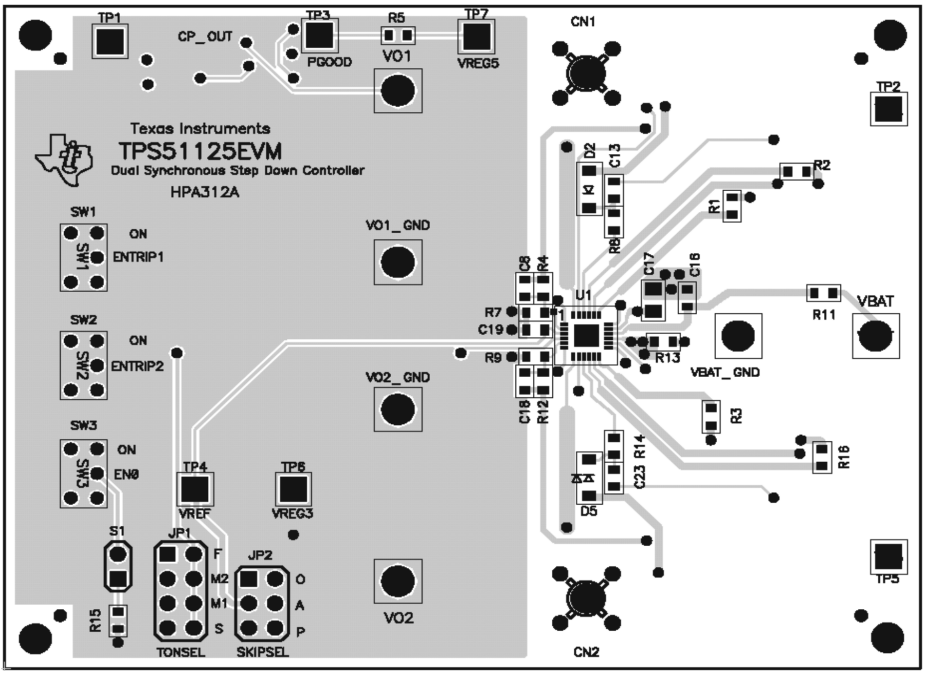

Figure 7. Top Layer Routing

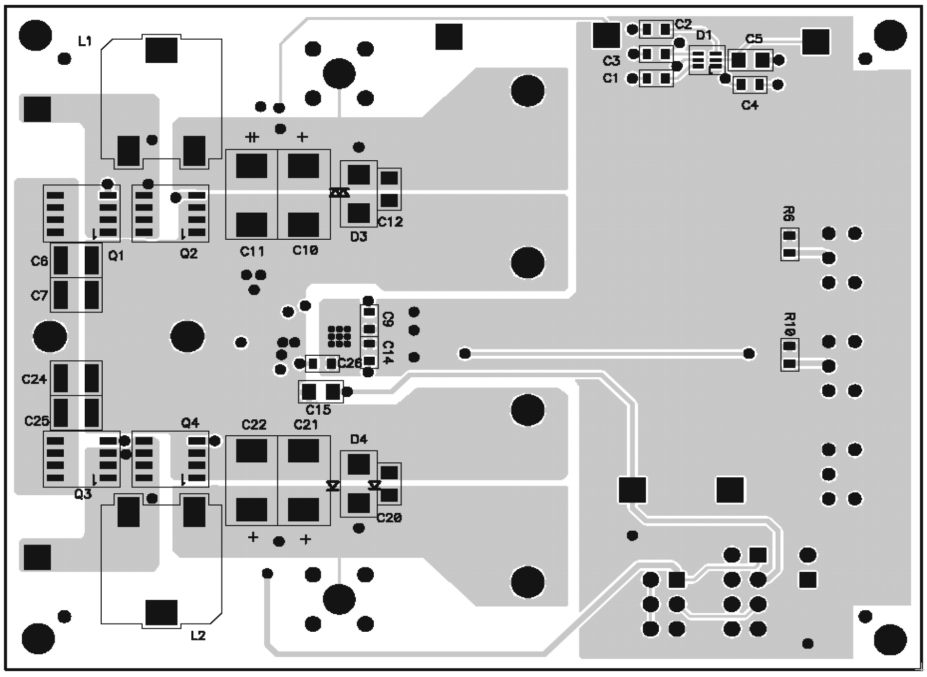

Figure 8. Bottom Layer Routing

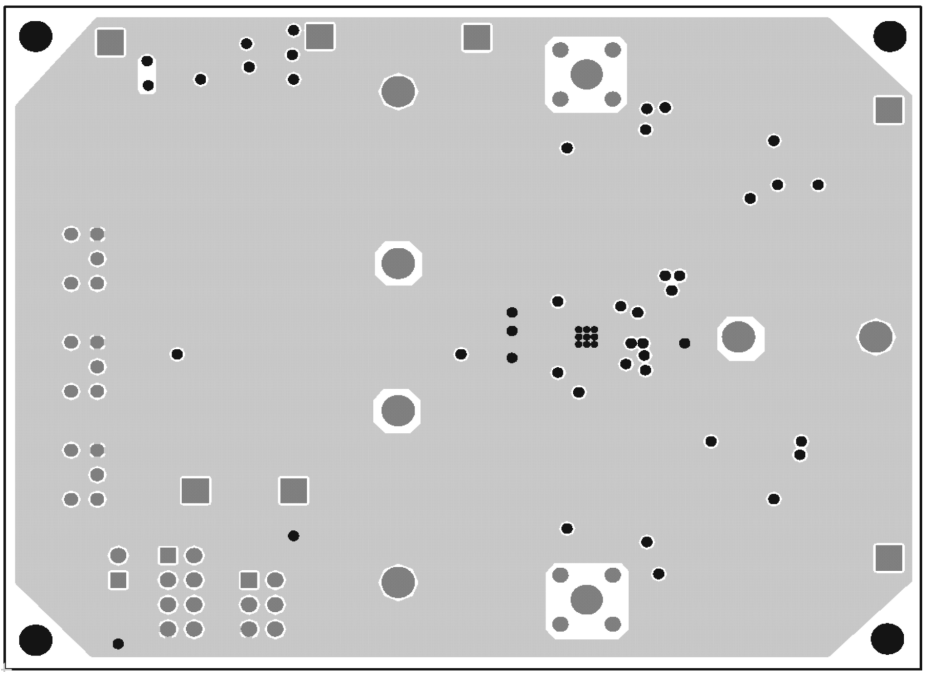

Figure 9. Inner Layer 1

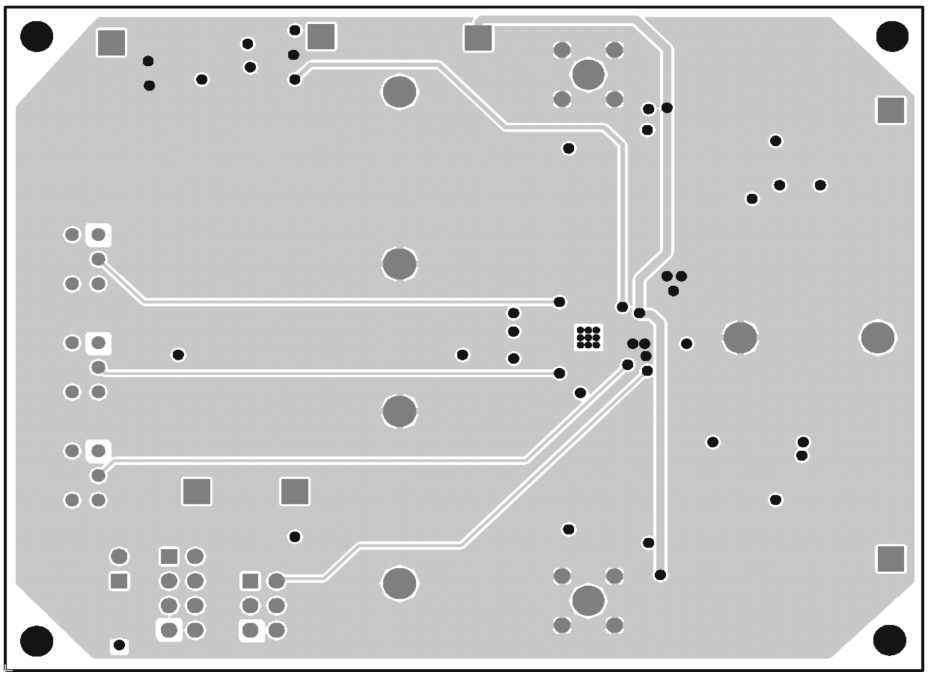

Figure 10. Inner Layer 2

7 List of Materials

List of materials for the TPS51125-EVM.

Table 5. TPS51125 Bill of Materials

RERERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1, C2, C3, C4, C13, C23	6	Capacitor, Ceramic, 0.1 µF, 50 V, X5R, 10%	0603	muRata	GRM188B31H104K
C10, C21	0	Capacitor	7.3 × 4.3 mm	Any	Any
C11, C22	2	Capacitor, POS, 330 µF, 6.3 V, 25 mΩ, 20%	7.3 × 4.3 mm	SANYO	6TPE330ML
C12, C20	0	Capacitor	0805	Any	Any
C15, C17	2	Capacitor, Ceramic, 10 µF, 6.3 V, X5R, 10%	0805	TDK	C2012X5R0J106K
C19	1	Capacitor, Ceramic, 220 nF, 16 V, X5R, 10%	0603	muRata	GRM188B31C224K
C5	1	Capacitor, Ceramic, 1 µF, 25 V, X5R, 10%	0805	TDK	C2012X7R1E105K
C6, C7, C24, C25	4	Capacitor, Ceramic, 10 µF, 25 V, BJ, M	1210	Taiyo Yuden	TMK325BJ106MM
C8, C9, C14, C16, C18, C26	0	Capacitor	0603	Any	Any
CN1, CN2	2	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.2	Tektronix	131-4244-00
D1	1	Diode, Schottky Barrier Array, 40 mA, 40 V	SOT363	Diodes	BAS40DW-04
D2, D5	0	Diode, Schottky, 0.5 A, 30 V	SOD-123	Any	Any
D3, D4	2	Diode, Schottky, 3 A, 20 V	SMA	Rohm	RSX501L(A)-20
JP1	1	Header, 2×4-pin, 100 mil spacing (36-pin strip)	0.20 × 0.40 inch	Sullins	PTC36DAAN
JP2	1	Header, 2×3-pin, 10 mil spacing (36-pin strip)	0.20 × 0.30 inch	Sullins	PTC36DAAN
L1, L2	2	Inductor, 3.3 µH, 14 A, 7.3 mΩ	0.425 × 0.45 inch	Toko	FDA1055-3R3M
Q1, Q3	2	MOSFET, N-channel, 30 V, 11 A, 9.1 mΩ	SO8	IR	IRF7821
Q2, Q4	2	MOSFET, N-channe,l 30 V, 11 A, 12.5 mΩ	SO8	Fairchild	FDS6690AS
R1, R3, R8, R11, R13, R14	6	Resistor, Chip, 0 Ω, 1/16 W, 1%	0603	Std	Std
R12	1	Resistor, Chip, 13 kΩ, 1/16W, 1%	0603	Std	Std
R15	1	Resistor, Chip, 620 kΩ, 1/16W, 1%	0603	Std	Std
R2, R16	2	Resistor, Chip, 5.1 Ω, 1/16W, 1%	0603	Std	Std
R4	1	Resistor, Chip, 30 kΩ, 1/16W, 1%	0603	Std	Std
R5	1	Resistor, Chip, 100 kΩ, 1/16W, 1%	0603	Std	Std
R6, R10	2	Resistor, Chip, 130 kΩ, 1/16W, 1%	0603	Std	Std
R7, R9	2	Resistor, Chip, 20 kΩ, 1/16W, 1%	0603	Std	Std
S1	1	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.1 inch × 2	Sullins	PTC36SAAN
SW1, SW2, SW3	3	Switch, ON-ON mini toggle	7.0 × 4.5 mm	Nikkai	G-12AP
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	Test point, yellow, through-hole	0.125 × 0.125 inch	Keystone	5014
U1	1	Dual Synchronous Step-Down ControllerWith OOA Operation and 100-mA LDO	QFN-24	TI	TPS51125RGE
VBAT_GND, VBAT, VO1, VO2, VO1_GND, VO2_GND	6	Pin, wiring terminal	0.12(D) × 0.4 inch	Mill Max	3138-2-00-15-00-00-080
	3	Shunt, 2POs, gold	0.100 × 0.200 inch	Molex	15-29-1025
	4	Standoff M/F hex 4-40 nylon	0.625 inch	Keystone	4803
	4	Nut hex 4-40 nylon	0.25 inch	Building Fasteners	NY HN 440

8 References

TPS51125 Datasheet, Dual-Synchronous Buck Controller (SLUS786)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.4 V to 16 V and the output voltage range of 2.3 V to 4.4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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